CHIP ELECTRONIC COMPONENT AND MANUFACTURE THEREOF

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Abstract

PROBLEM TO BE SOLVED: To provide a chip electronic component of side-mounting type and its manufacturing method, where the electronic component is surely enhanced in mounting strength and electrical connection reliability and self-aligned, when it is mounted on a motherboard.
SOLUTION: A board 1 where an LED element 3 is assembled is sealed with a rectangular parallelopipedic molded epoxy resin 5. The LED element 3 is mounted on a board 1 to serve as a side light-emitting type element (the direction of light is shown by the arrow in figure), and the board 1 is so set in the resin molded body 5 as to face the front side of the molded body 5. Electrodes 6 provided on the surface of the molded body 5 are so arranged on the upper and lower edges of the molded body 5 for facedown bonding. The board electrodes and the molded body electrodes 6 are electrically connected together with electrodes that come out of the dicing face of the molded body 5 and a plating film formed on the dicing face.

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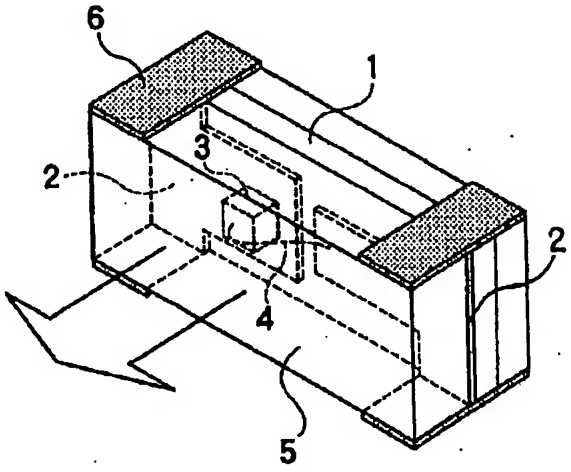
(54)【発明の名称】　チップ電子部品およびその製造方法

(57)【要約】
【課題】　側面型チップ電子部品をマザーボードに実装接続する場合に、取り付け強度や電気的接続が確保され、半田付け時にセルフ・アライメントが働くような構造を持つ前記チップ電子部品及びその製造方法を提供すること。
【解決手段】　ＬＥＤ素子３を組み立てた基板１を封止し全体を直方体にエポキシ樹脂５で成形してモールド体をなす。側面発光型を構成すべく（発光方向は図示の矢印）ＬＥＤ素子３がマウントされる基板１をモールド体の側面に向く関係におく。モールド体の表面に付けられた電極６の配置はフェイスダウンボンディングするために、モールド体の上下面の両端部に沿う配置をとる。基板側電極とモールド体電極６の導電は、モールド体のダイシング面に露出させる電極とこの面に形成されるメッキ膜により確保する。



【特許請求の範囲】
【請求項１】　導電層を設けた絶縁基板に半導体素子をマウントし、該絶縁基板と半導体素子を樹脂封止した素子モールド体であって、その外面に該絶縁基板の端面が導電層の一部とともに露出する素子モールド体と、前記素子モールド体の外面に前記導電層に導電接続するように設けた電極とを有するチップ電子部品。
【請求項２】　前記電極を設ける面を、前記半導体素子がマウントされた前記絶縁基板の面に対して略垂直をなすようにした前記素子モールド体の側面としたことを特徴とする請求項１記載のチップ電子部品。
【請求項３】　前記絶縁基板にマウントされる素子を半導体発光素子としたことを特徴とする請求項１又は２記載のチップ電子部品。
【請求項４】　絶縁基板に半導体素子に応じた形状の導電層の単位パターンの繰り返しパターンを形成し、前記パターンを形成した絶縁基板に複数の半導体素子を組み立て、前記絶縁基板及び該絶縁基板に組み立てた半導体素子を樹脂モールドし、このモールド体を切断してその切断面に前記パターンの端部断面を露出させる切り出しを行い、前記切り出しにより露出させたパターンの端部断面を含む切断面を同一面に配置し前記モールド体から切り出されたモールド体をさらに樹脂モールドして素子モールド体を形成し、この素子モールド体において同一面に配置された前記切断面を含む全面に導電金属のメッキを施し、前記メッキを施した面から不要なメッキ部分をパターニング除去し、前記メッキのパターニング除去を行った素子モールド体を個々のチップ電子部品に分割することを特徴とするチップ電子部品の製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、側面型チップ電子部品に関し、より詳細には、チップ電子部品の樹脂モールド体の表面に電極を形成してなるチップ電子部品及びその製造方法に関し、特に例えば、ＬＥＤ、フォトカプラ、フォトトランジスタ等の光半導体デバイスに有効に適用し得るものである。
【０００２】
【従来の技術】従来の側面発光型チップＬＥＤの１例を図１２に斜視図にて示す。図１２において、側面発光型チップＬＥＤ２０は、マザーボード２１に組み付け、側面発光する状態に載置した状態にある。側面発光型チップＬＥＤ２０そのものは、ほぼ直方体状の絶縁基板１１の一面にパターニングされた導電膜からなる電極１２に半導体発光層を有するＬＥＤ素子１３をマウントし、さらにＬＥＤ素子１３を保護しかつ光を所定の方向に導くための機能を持つ封止樹脂１５で絶縁基板１１のＬＥＤ素子１３が載置する面の一部を覆っている。図示の従来例で採用されている基板の電極構造は、ＬＥＤ素子１３がマウントされている面からその裏面にわたる４側面に電極１２が設けられている。そして、絶縁基板１１の両端の電極１２は、基板１１のＬＥＤ素子１３がマウントされている面をマザーボード２１に対して垂直になるように半田接続されている。従って、チップＬＥＤ２０のマザーボード２１と相対する基板１１の面には電極が存在しない。これは、一枚の絶縁基板の周囲面に複数チップ分の電極を形成した後、ダイシングにより各チップを切り出し、切り出された面をマザーボード２１に相対するように実装するからである。
【０００３】このように従来の電極構造では、取り付け強度が弱く、接触によりチップ部品の脱落が起きる危険性がある。特に、側面発光型チップＬＥＤの場合には、マザーボードの端部に取り付けられることが多いので、ボードを取り扱っている時に接触により脱落等が起きる危険性が高い。さらに、マザーボードの配線面に対するチップＬＥＤ側の面には電極が設けられていないことから、半田付け時にセルフ・アライメントが働かず取り付け後の位置精度が出ない、或いは接続不良が起きるといった問題や、小型のチップ部品の場合に半田付ができなかったり、マンハッタン現象でチップが起立するという問題が生じる。
【０００４】
【発明が解決しようとする課題】本発明は、上述した従来の側面型チップ電子部品における問題点に鑑みてなされたものであって、その目的は、前記電子部品をマザーボードに実装接続する場合に、取り付け強度や電気的接続が確保され、半田付け時にセルフ・アライメントが働くような構造を持つ前記チップ電子部品及びその製造方法を提供することにある。
【０００５】
【課題を解決するための手段】請求項１の発明は、導電層を設けた絶縁基板に半導体素子をマウントし、該絶縁基板と半導体素子を樹脂封止した素子モールド体であって、その外面に該絶縁基板の端面が導電層の一部とともに露出する素子モールド体と、前記素子モールド体の外面に前記導電層に導電接続するように設けた電極とを有するチップ電子部品を構成する。
【０００６】請求項２の発明は、請求項１記載のチップ電子部品において、前記電極を設ける面を、前記半導体素子がマウントされた前記絶縁基板の面に対して略垂直をなすようにした前記素子モールド体の側面としたことを特徴とするものである。
【０００７】請求項３の発明は、請求項１又は２記載の側面型チップ電子部品において、前記絶縁基板にマウントされる素子を半導体発光素子としたことを特徴とするものである。
【０００８】請求項４の発明は、絶縁基板に半導体素子に応じた形状の導電層の単位パターンの繰り返しパターンを形成し、前記パターンを形成した絶縁基板に複数の半導体素子を組み立て、前記絶縁基板及び該絶縁基板に

組み立てた半導体素子を樹脂モールドし、このモールド体を切断してその切断面に前記パターンの端部断面を露出させる切り出しを行い、前記切り出しにより露出させたパターンの端部断面を含む切断面を同一面に配置し前記モールド体から切り出されたモールド体をさらに樹脂モールドして素子モールド体を形成し、この素子モールド体において同一面に配置された前記切断面を含む全面に導電金属のメッキを施し、前記メッキを施した面から不要なメッキ部分をパターニング除去し、前記メッキのパターニング除去を行った素子モールド体を個々のチップ電子部品に分割することを特徴とするチップ電子部品の製造方法を構成する。

【０００９】

【発明の実施の形態】以下、本発明によるチップ電子部品及びその製造方法の実施の形態を添付する図面に基づいて説明する。図１は、本発明によるチップ電子部品の一実施形態例の側面発光型チップＬＥＤの外観を斜視図にて示す。また、図２及び図３は、図１に示される側面発光型チップＬＥＤの平面図及び側面図をそれぞれ示す。本実施形態のチップＬＥＤは、両端部に対向する一対の導電層２，２を設けた平面視矩形状絶縁基板１と、絶縁基板１の一方の導電層２上に下面を導体ペーストでマウントされ、上面を他方の導電層２とワイヤ４で電気的に接続されたＬＥＤ素子３とをエポキシ樹脂５で封止し、図１に示すように、全体をほぼ直方体に成形した樹脂モールド体をなす。ここでは、側面発光型を構成すべく（図１は側面発光状態にあり、発光方向を図示の矢印にて示す）、樹脂モールド体の側面が発光面となるようにＬＥＤ素子３をマウントする基板１を発光面となる側面に平行な関係におき、素子モールド体を成形する。

【００１０】また、素子モールド体の表面には、電極６を設ける。電極６の配置は、図１乃至３に示すように、マザーボード側の配線（図示せず）にボンディングするために、素子モールド体の上下面（すなわち、発光面をなす側面に対する上下面）とし、この実施形態においては、向かい合う上下面の両端部に沿い配置する。このように設けられる電極６には絶縁基板１の導電層２を導電接続しなければならない。その接続方法は、絶縁基板１に設けた導電層２を素子モールド体の上下面に絶縁基板１の端面とともに露出させ、露出させた導電層２を含む面に電極６を形成することにより行う。なお、本実施形態では樹脂モールド体の上下両面に電極６を設けているが、単一のＬＥＤ素子を載せる場合、電極は基本的にいずれかの面に一対あればよい。また、極性を選択してマザーボード上に実装する必要がある場合には、共通の電極を上下両面にそれぞれ設け、面を選択して用いる。

【００１１】上記した側面発光型チップＬＥＤは、樹脂モールド体の下面に必要な大きさの両極用の電極を設けているので、マザーボード側の配線にボンディングする場合に、両電極がマザーボード側の配線パターン面に面同士で接触することになる。そのため、取り付け強度や電気的接続が十分に確保され、また、半田付けの際にセルフアライメントが働くから、位置精度を出すことができ、接続不良や、マンハッタン現象でチップの起立が発生するという問題が起きることがなく、半田付けの信頼性が向上する。また、マザーボードの端部への実装を必要とする側面発光型チップＬＥＤにおいて、従来の不完全な接続方法を採ったために起きていた接触によるチップの脱落を無くすことができる。

【００１２】次に、本発明によるチップ電子部品の製造方法の一実施形態として、上記で示した側面発光型チップＬＥＤの作成法について、以下にその説明をする。図４ないし図１１は、本実施形態の概要を説明するための図で、作成過程で加工・処理されるチップＬＥＤの状態を順に表す図である。なお、同図中においてチップＬＥＤの構成要素には図１乃至３と共通の参照番号を付している。図４ないし図１１に基づき、以下に本実施形態の側面発光型チップＬＥＤの作成の工程に従い、詳細に説明する。なお、この実施形態では、図４に示すように、導電層２を絶縁基板１の片面上のみに形成した例を示しているが、基板１の両面に側面を介して亘るように形成してもよく、この場合、基板１の両面にＬＥＤ素子を組み立てることも出来る。

【００１３】（素子組立工程：図４参照）ＬＥＤ素子３を絶縁基板１へ組み立てる工程で、この例では、絶縁基板１上に縦及び横方向に整列した繰り返しパターン配列で形成されている複数チップ分の導電層２の各素子マウント部に、ＬＥＤ素子３を銀ペースト等によりダイボンディングし、さらに、ＬＥＤ素子３のもう一方の電極と前記マウント部と対向する導電層２との間に、金線のワイヤ４によりワイヤボンディングを行う工程である。

【００１４】（樹脂封止工程：図５参照）この工程では、前工程で組み立てた絶縁基板１上のＬＥＤ素子３及びボンディングしたワイヤ４まわりを透光性の樹脂でモールドし、少なくともＬＥＤ素子３とワイヤ４部分を封止する。この樹脂封止工程を終了した時点における状態を図５に示す。ここでは、ＬＥＤ素子３及びボンディングしたワイヤ４まわりをモールドした樹脂５が凸部状に横方向に一定の高さで連なり、樹脂５の凸部と凸部の間は、樹脂モールドしないために導電層２が露出している。

【００１５】（樹脂封止基板切り出し工程：図６参照）この工程は、前の樹脂封止工程で封止された基板を切り出す工程で、ダイサー等の手段を用い導電層２の縦方向の配列に沿い、かつ樹脂封止工程で封止を必要としたＬＥＤ素子３及びボンディングしたワイヤ４まわりが保存されるように、素子列の中間（図５のＡ－Ａ破線）を切断してバー状の素子列を切り出す。図６は、この樹脂封止基板切り出し工程を終了した時点における状態を示す。図示のように、前工程で導電層２は、繰り返しパタ

ーンを縦及び横方向に連続パターンの形態をとるように形成しているので、この切り出しにより、横方向に並ぶ素子３の間で連続していた導電層２が切り離され、導電層２の端部断面が露出される。

【００１６】（樹脂モールド工程：図７、図８参照）この工程は、前の樹脂封止基板切り出し工程にて切り出された素子列を配列し直し、全体を樹脂モールドする工程である。この工程では、先ず、図７に示すように、切り出された各素子列を横置きにし、かつ各素子列の切断面を同一平面上に置き、さらに各素子列を縦方向に素子の単位で整列させるようにして各素子列を重ね配列し直す。このように配列することにより、後述する各チップＬＥＤへのダイシングによる分割を可能とする次に、この様な配列を保って上下を成形金型（図示せず）で締め付け、成形金型と各素子列とにより作られるキャビテイに透光性の樹脂５ｍを充填し、固化させ樹脂モールドする。図８は、この樹脂モールド工程を終了した時点における状態を示す。図示のように、図７における各素子列間の空間に樹脂５ｍが充填され、全体として直方体のモールド体をなしている。なお、図８の状態にあるモールド体の上面（及び／又は下面）は、図７の配置を取った時の各素子列の切断面を維持していること、つまり、樹脂封止基板切り出し工程で切り出された素子列の切断面内に導電層２の端部断面を露出していることが必要である。従って、樹脂モールド工程で露出していた導電層２が樹脂５ｍで覆われた場合又はより確実に露出させたい場合には、露出させる工程（例えば、研磨による）を行えばよい。

【００１７】（導電金属膜メッキ工程：図９参照）この工程は、前工程の樹脂モールド工程で得られた直方体状のモールド体の絶縁基板１の切断面が露出する上面及び／又は下面の全面に導電金属膜６、例えば、Ｃｕ・Ｎｉ合金に加えフラッシュ金のメッキを設ける。この時、モールド体の上面（及び／又は下面）に露出している導電層２に導電金属膜６が接触し、両者間が導電接続する。

【００１８】（導電金属膜除去工程：図１０参照）この工程は、前の導電金属膜メッキ工程で行ったメッキ面から不要な部分を除去する工程である。前の工程で直方体状のモールド体の上面（及び／又は下面）の全面に導電金属膜６がメッキされているので、各ＬＥＤ素子３が電気的に接続された対向する一対の導電層２はこの導電金属膜６により導通された状態にある。そこで、エッチング、研磨等により導電金属膜６を帯状にを除去することにより各素子列の各ＬＥＤ素子３の対向する一対の導電層２を一度に分離する。すなわち、先の工程で素子列を整列させており、導電金属膜６と接続する素子列側の各ＬＥＤ素子３の導電層２との接続点は直線上に並んでいるので、この工程が終わった状態を示す図１０に示すように、縦方向に帯状に導電金属膜６を残し、それ以外の部分は除去する。

【００１９】（ダイシング工程：図１１参照）この工程は、側面発光型チップＬＥＤとしての個々の部品に分割する工程でダイサーにより素子分割を行う。縦方向については、前工程で帯状に残した導電金属膜６の幅の中央をカットラインとし、横方向についても等しいピッチで所定の位置をカットすることにより、図１乃至３に示されたチップＬＥＤを得ることが出来る。ここでは、メッキ工程で形成された導電金属膜６の幅の中央をカットラインとし、個々のチップＬＥＤへの分割を行っているので、分割後のチップＬＥＤの向かい合う上下面における導電金属膜６による電極の配置は、両端部に沿う配置をとることになり、チップＬＥＤの構造に図１乃至３に示すような特徴をもたらす。

【００２０】

【発明の効果】本発明によると、端部に導電層を有する絶縁基板に素子を載せた組立部品の樹脂モールド体の外面に絶縁基板の端面を前記導電層とともに露出させ、露出した導電層の一部乃至全部を含むように樹脂モールド体の外面に電極を形成することにより、電極と導電層の導電接続を確保してチップ電子部品を横置き実装に対応する構成としたため、チップ電子部品を横向きに実装した時、樹脂モールド体の下面に形成した電極がマザーボード側の配線パターン面に面同士で接触するので、取り付け強度や電気的接続が十分に確保される。さらに、電極と配線とを面同士の接触で半田による接続を行う場合に、半田付け時にセルフアライメントが働くことから、従来の例えば側面発光型チップＬＥＤにおいて問題であった取り付け後の位置精度、接続不良、或いはマンハッタン現象でチップの起立が発生するという問題が生じることがない。また、しばしばマザーボードの端部への実装が必要である側面発光型チップＬＥＤへ本発明を適用することにより、従来の側面発光型チップＬＥＤを実装した場合に起きていた不完全な接続によるチップの脱落を少なくすることが可能となる。また、本発明の方法により、前記特徴を備えた側面型チップ電子部品を容易かつ効率良く作成することが出来る。

【図面の簡単な説明】

【図１】本発明による側面発光型チップＬＥＤの一実施形態を示す斜視図である。

【図２】図１に示される側面発光型チップＬＥＤの平面図である。

【図３】図１に示される側面発光型チップＬＥＤの側面図である。

【図４】側面発光型チップＬＥＤの製造工程を説明する図で、素子組立工程における製品の状態を示す。

【図５】側面発光型チップＬＥＤの製造工程を説明する図で、樹脂封止工程における製品の状態を示す。

【図６】側面発光型チップＬＥＤの製造工程を説明する図で、樹脂封止基板切り出し工程における製品の状態を示す。

【図7】側面発光型チップＬＥＤの製造工程を説明する図で、樹脂モールド工程における素子列の配置状態を示す。

【図8】側面発光型チップＬＥＤの製造工程を説明する図で、導電金属膜メッキ工程における製品の状態を示す。

【図9】側面発光型チップＬＥＤの製造工程を説明する図で、導電金属膜除去工程における製品の状態を示す。

【図10】側面発光型チップＬＥＤの製造工程を説明する図で、導電金属膜除去工程における製品の状態を示す。

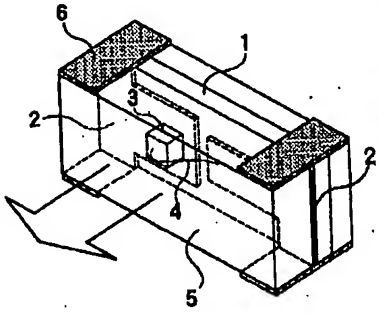
【図11】側面発光型チップＬＥＤの製造工程を説明する図で、ダイシング工程における製品の状態を示す。

【図12】従来の側面発光型チップＬＥＤの１例をマザーボードへのマウント状態にて示す斜視図である。

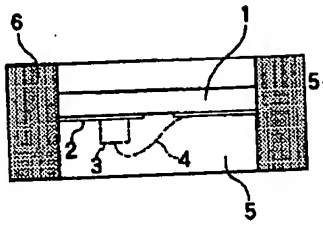
【符号の説明】

1、11…絶縁基板、
2、12…導電層、
3、13…ＬＥＤ素子、
4…ワイヤ、
5、15…樹脂、
6…電極（導電金属膜）、
20…側面発光型チップＬＥＤ、
21…マザーボード。

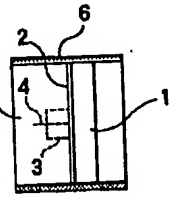
【図1】



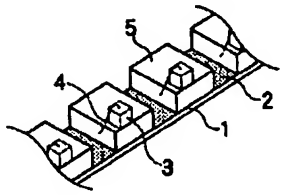
【図2】



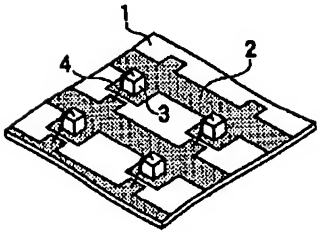
【図3】



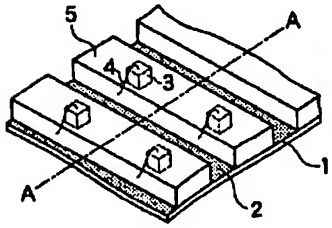
【図6】



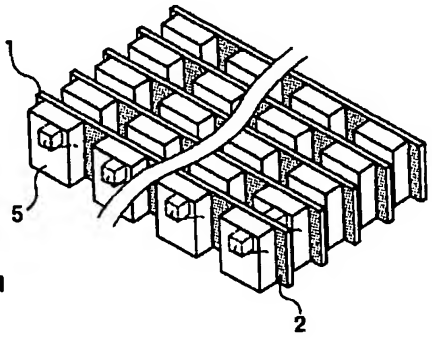
【図4】



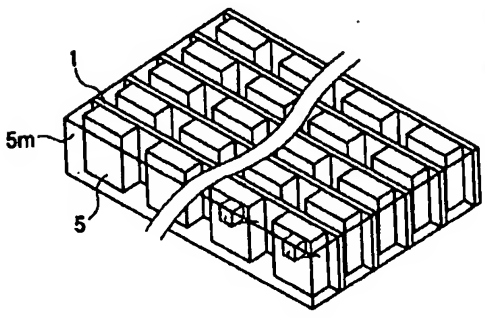
【図5】



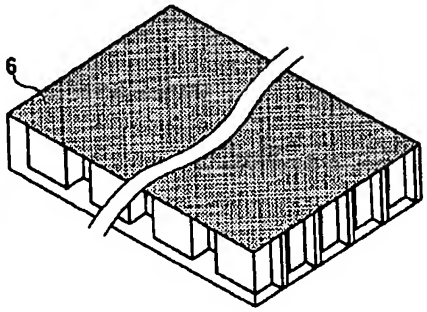
【図7】



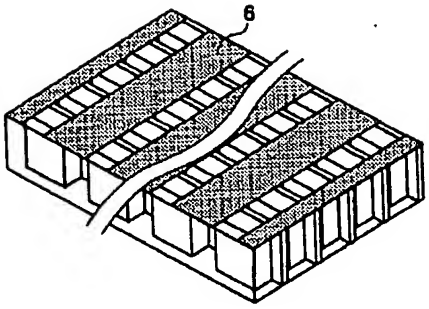
【図8】



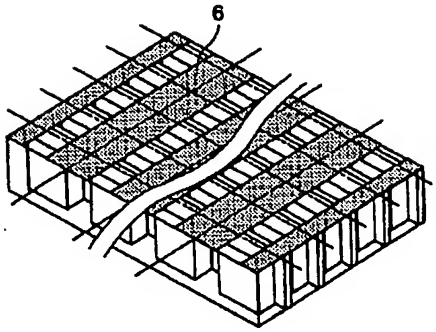
【図9】



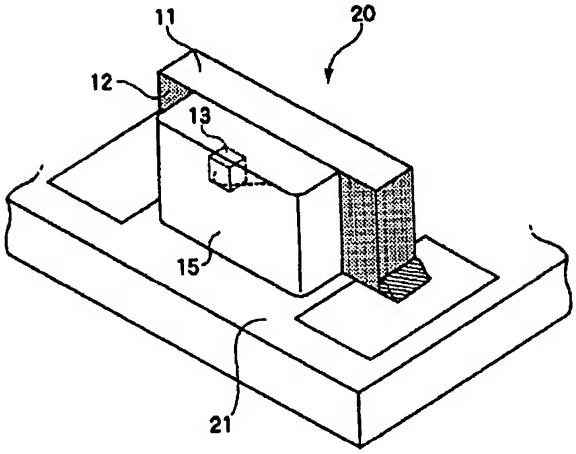
【図10】



【図11】



【図12】



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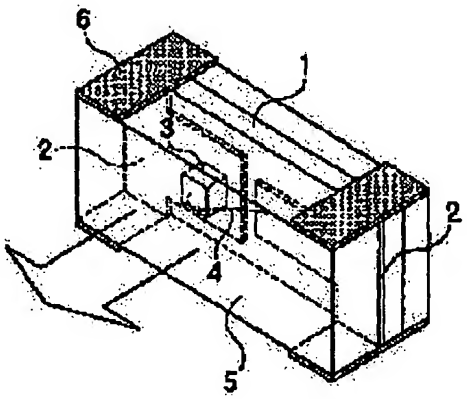
(54) CHIP ELECTRONIC COMPONENT AND MANUFACTURE THEREOF

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a chip electronic component of side-mounting type and its manufacturing method, where the electronic component is surely enhanced in mounting strength and electrical connection reliability and self-aligned, when it is mounted on a motherboard.

SOLUTION: A board 1 where an LED element 3 is assembled is sealed with a rectangular parallelopipedic molded epoxy resin 5. The LED element 3 is mounted on a board 1 to serve as a side light-emitting type element (the direction of light is shown by the arrow in figure), and the board 1 is so set in the resin molded body 5 as to face the front side of the molded body 5. Electrodes 6 provided on the surface of the molded body 5 are so arranged on the upper and lower edges of the molded body 5 for facedown bonding. The board electrodes and the molded body electrodes 6 are electrically connected together with electrodes that come out of the dicing face of the molded body 5 and a plating film formed on the dicing face.



LEGAL STATUS

[Date of request for examination]

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[Date of final disposal for application]

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* NOTICES *

CLAIMS

[Claim(s)]
[Claim 1] Chip electronic parts which have the element mould object which is an element mould object which mounted the semiconductor device on the insulating substrate which prepared the conductive layer, and carried out the resin seal of the semiconductor device to this insulating substrate, and the end face of this insulating substrate exposes to the external surface with a part of conductive layer, and the electrode prepared so that it might connect conductively to the external surface of the aforementioned element mould object at the aforementioned conductive layer.
[Claim 2] Chip electronic parts according to claim 1 characterized by considering as the side of the aforementioned element mould object in which the abbreviation perpendicular was made to the field of the aforementioned insulating substrate where the aforementioned semiconductor device was mounted in the field in which the aforementioned electrode is prepared.
[Claim 3] Chip electronic parts according to claim 1 or 2 characterized by making into a semiconductor light emitting device the element mounted on the aforementioned insulating substrate.
[Claim 4] The repeat pattern of the unit pattern of the conductive layer of a configuration according to the semiconductor device is formed in an insulating substrate. The resin mould of the semiconductor device which assembled two or more semiconductor devices to the insulating substrate in which the aforementioned pattern was formed, and was assembled to the aforementioned insulating substrate and this insulating substrate is carried out. Logging which this mould object is cut [logging] and exposes the edge cross section of the aforementioned pattern to the cutting plane is performed. Carry out the resin mould of the mould object which has arranged the cutting plane containing the edge cross section of the pattern exposed by the aforementioned logging to the same field, and was cut down from the aforementioned mould object further, and an element mould object is formed. An electric conduction metal is plated all over the aforementioned cutting plane arranged in this element mould object in the same side being included. The manufacture method of the chip electronic parts which carry out patterning removal of the plating portion unnecessary from the field which gave the aforementioned plating, and are characterized by dividing into each chip electronic parts the element mould object which performed patterning

removal of the aforementioned plating.

[Translation done.]

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention can be especially applied more to a detail about side type chip electronic parts about the chip electronic parts which come to form an electrode in a front face and its manufacture method of a resin mould object of chip electronic parts effective in optical semiconductor devices, such as Light Emitting Diode, a photo coupler, and a photo transistor, for example.
[0002]
[Description of the Prior Art] A perspective diagram shows one example of the conventional side luminescence type chip Light Emitting Diode to drawing 12 . In drawing 12 , the side luminescence type chip Light Emitting Diode 20 is in the state where attached to the mother board 21 and it laid in the state of carrying out side luminescence. Side luminescence type chip Light Emitting Diode20 themselves are wearing a part of field which the Light Emitting Diode element 13 of an insulating substrate 11 lays by the closure resin 15 with the function for mounting the Light Emitting Diode element 13 which has a semiconductor luminous layer on the electrode 12 which consists of an electric conduction film by which patterning was mostly carried out to the whole surface of the rectangular parallelepiped-like insulating substrate 11, and protecting the Light Emitting Diode element 13 further, and drawing light in the predetermined direction. As for the electrode structure of the substrate adopted in the conventional example of illustration, the electrode 12 is formed in the 4 sides ranging from the field to the rear face where the Light Emitting Diode element 13 is mounted. And solder connection of the electrode 12 of the ends of an insulating substrate 11 is made so that it may become perpendicular to a mother board 21 about the field where the Light Emitting Diode element 13 of a substrate 11 is mounted. Therefore, an electrode does not exist in the field of the substrate 11 which faces the mother board 21 of a chip Light Emitting Diode 20. This is because each chip is started by dicing, and the started field is mounted so that a mother board 21 may be faced after forming the electrode for two or more chips in the circumference side of the insulating substrate of one sheet.
[0003] Thus, with the conventional electrode structure, installation intensity is weak and there is a danger that defluxion of a chip will occur by contact. The

danger that defluxion etc. will occur by contact especially while dealing with the board, since it is attached in the edge of a mother board in many cases in the case of the side luminescence type chip Light Emitting Diode is high. Furthermore, since the electrode is not prepared in the field by the side of the chip Light Emitting Diode to the wiring side of a mother board, the problem that self-alignment does not work, and the position precision after installation does not come out, or a faulty connection occurs at the time of soldering, and the problem that soldering is impossible in the case of a small chip, or a chip stands up by the Manhattan phenomenon arise.

[0004]

[Problem(s) to be Solved by the Invention] this invention is made in view of the trouble in the conventional side type chip electronic parts mentioned above, installation intensity and electrical installation are secured and the purpose is in offering the aforementioned chip electronic parts with structure which self-alignment commits at the time of soldering, and its manufacture method, when making mounting connection of the aforementioned electronic parts at a mother board.

[0005]

[Means for Solving the Problem] Invention of a claim 1 mounts a semiconductor device on the insulating substrate which prepared the conductive layer, is the element mould object which carried out the resin seal of the semiconductor device to this insulating substrate, and constitutes the chip electronic parts which have the element mould object which the end face of this insulating substrate exposes to the superficies with a part of conductive layer, and the electrode prepared so that it might connect conductively to the superficies of the aforementioned element mould object at the aforementioned conductive layer.

[0006] Invention of a claim 2 is characterized by considering as the side of the aforementioned element mould object in which the abbreviation perpendicular was made to the field of the aforementioned insulating substrate where the aforementioned semiconductor device was mounted in the field in which the aforementioned electrode is prepared in chip electronic parts according to claim 1.

[0007] Invention of a claim 3 is characterized by making into a semiconductor light emitting device the element mounted on the aforementioned insulating substrate in side type chip electronic parts according to claim 1 or 2.

[0008] Invention of a claim 4 forms the repeat pattern of the unit pattern of the conductive layer of the configuration according to the semiconductor device in an insulating substrate. The resin mould of the semiconductor device which assembled two or more semiconductor devices to the insulating substrate in which the aforementioned pattern was formed, and was assembled to the aforementioned insulating substrate and this insulating substrate is carried out. Logging which this mould object is cut [logging] and exposes the edge cross section of the aforementioned pattern to the cutting plane is performed. Carry out the resin mould of the mould object which has arranged the cutting plane containing the edge cross section of the pattern exposed by the aforementioned logging to the same field, and was cut down from the aforementioned mould object further, and an element mould object is formed. An electric conduction metal is plated all over

the aforementioned cutting plane arranged in this element mould object in the same side being included. The manufacture method of the chip electronic parts which carry out patterning removal of the plating portion unnecessary from the field which gave the aforementioned plating, and are characterized by dividing into each chip electronic parts the element mould object which performed patterning removal of the aforementioned plating is constituted.

[0009]

[Embodiments of the Invention] Hereafter, it explains based on the drawing which appends the gestalt of operation of the chip electronic parts by this invention, and its manufacture method. Drawing 1 shows the appearance of the side luminescence type chip Light Emitting Diode of the example of 1 operation gestalt of the chip electronic parts by this invention with a perspective diagram. Moreover, drawing 2 and drawing 3 show the plan and side elevation of the side luminescence type chip Light Emitting Diode which are shown in drawing 1 , respectively. one conductive-layer 2 top of the plane view rectangle-like insulating substrate 1 which formed the conductive layers 2 and 2 of the couple to which the chip Light Emitting Diode of this operation gestalt counters both ends, and an insulating substrate 1 — an inferior surface of tongue — a conductor — as it mounts with a paste, and the Light Emitting Diode element 3 to which the upper surface was electrically connected with the conductive layer 2 and wire 4 of another side is closed by the epoxy resin 5 and shown in drawing 1 , the resin mould object which fabricated the whole in the rectangular parallelepiped mostly is made Here, that a side luminescence type should be constituted (drawing 1 is in a side luminescence state, and shows the luminescence direction by the arrow of illustration), the substrate 1 which mounts the Light Emitting Diode element 3 is set in a relation parallel to the side used as a luminescence side so that the side of a resin mould object may turn into a luminescence side, and an element mould object is fabricated.

[0010] Moreover, an electrode 6 is formed in the front face of an element mould object. As shown in drawing 1 or 3, in order to carry out bonding to the wiring by the side of a mother board (not shown), arrangement of an electrode 6 considers as the vertical side (namely, vertical side over the side in which a luminescence side is made) of an element mould object, and is arranged in this operation form along the both ends of the vertical side which faces each other. Thus, you have to connect the conductive layer 2 of an insulating substrate 1 conductively to the electrode 6 prepared. The connection method is performed by forming an electrode 6 in the field containing the conductive layer 2 to which it was made to expose to the vertical side of an element mould object with the end face of an insulating substrate 1, and the conductive layer 2 prepared in the insulating substrate 1 was exposed. In addition, although the electrode 6 is formed in vertical both sides of a resin mould object with this operation form, when carrying a single Light Emitting Diode element, one pair of electrode should just be in one of fields fundamentally. Moreover, when it is necessary to choose polarity and to mount on a mother board, a common electrode is prepared in vertical both sides, respectively, and a field is chosen and used.

[0011] Since the above-mentioned side luminescence type chip Light Emitting

Diode has prepared the electrode for the two poles of a size required for the inferior surface of tongue of a resin mould object, when carrying out bonding to the wiring by the side of a mother board, two electrodes will contact the circuit pattern side by the side of a mother board in fields. Therefore, since installation intensity and electrical installation are fully secured and self-alignment works in the case of soldering, position precision can be taken out, neither a faulty connection nor the problem that standing up of a chip occurs by the Manhattan phenomenon occurs, and the reliability of soldering improves. Moreover, in the side luminescence type chip Light Emitting Diode which needs mounting to the edge of a mother board, defluxion of the chip by the contact which had occurred since the conventional imperfect connection method was taken can be lost.

[0012] Next, the explanation is given to below about the method of creating the side luminescence type chip Light Emitting Diode shown above as 1 operation gestalt of the manufacture method of the chip electronic parts by this invention. Drawing 4 or drawing 11 is drawing for explaining the outline of this operation gestalt, and is drawing which expresses in order the state of the chip Light Emitting Diode processed and processed in creation process. In addition, drawing 1 , or 3 and a common reference number is given to the component of Chip Light Emitting Diode all over this drawing. Based on drawing 4 or drawing 11 , it explains in detail according to the process of creation of the side luminescence type chip Light Emitting Diode of this operation gestalt below. In addition, although this operation gestalt shows the example in which the conductive layer 2 was formed only on one side of an insulating substrate 1 as shown in drawing 4 , you may form so that both sides of a substrate 1 may be covered through the side, and a Light Emitting Diode element can also be assembled to both sides of a substrate 1 in this case.

[0013] At the process assembled to an insulating substrate 1, the Light Emitting Diode element 3 (: refer to drawing 4 like an element erector) In this example In each element mounting section of the conductive layer 2 for two or more chips which aligned on the insulating substrate 1 at length and the longitudinal direction and which is repeatedly formed in the pattern array It is the process which carries out die bonding of the Light Emitting Diode element 3 with a silver paste etc., and performs wirebonding with the wire 4 of a gold streak further between another electrode of the Light Emitting Diode element 3, the aforementioned mounting section, and the conductive layer 2 that counters.

[0014] (Resin-seal process : refer to drawing 5) At this process, the mould of the circumference of the Light Emitting Diode element 3 on the insulating substrate 1 assembled at the last process and the wire 4 which carried out bonding is carried out by the resin of a translucency, and the Light Emitting Diode element 3 and wire 4 portion are closed at least. The state at the time of ending this resin-seal process is shown in drawing 5 . Here, the resin 5 which carried out the mould of the circumference of the Light Emitting Diode element 3 and the wire 4 which carried out bonding stood in a row in height fixed in the shape of heights in a longitudinal direction, and in order not to carry out the resin mould of between the heights of a resin 5, the conductive layer 2 has exposed it.

[0015] (Resin-seal substrate logging process : refer to drawing 6) This process is

a process which starts the substrate closed at the front resin-seal process, cuts the middle (A-A dashed line of drawing 5) of an element array, and cuts down a bar-like element array so that the circumference of the Light Emitting Diode element 3 which needed closure at the resin-seal process along with the lengthwise array of a conductive layer 2 using meanses, such as a dicer, and the wire 4 which carried out bonding may be saved. Drawing 6 shows the state at the time of ending this resin-seal substrate logging process. Like illustration, at a last process, since the conductive layer 2 forms the repeat pattern so that the gestalt of a continuation pattern may be taken in length and a longitudinal direction, the conductive layer 2 which was continuing between the elements 3 on a par with a longitudinal direction by this logging is separated, and the edge cross section of a conductive layer 2 is exposed.

[0016] (Resin mould process : refer to drawing 7 and drawing 8) This process is a process which rearranges the element array cut down at the front resin-seal substrate logging process, and carries out the resin mould of the whole. At this process, first, as are shown in drawing 7 , and each cut-down element array is carried out every width, and the cutting plane of each element array is put on a coplanar and each element array is further aligned in the unit of an element lengthwise, each element array is piled up and rearranged. thus, such [the degree which enables division by the dicing to each chip Light Emitting Diode later mentioned by arranging] an array — maintaining — the upper and lower sides — fabrication — metal mold (not shown) — binding tight — fabrication — the cavity made with metal mold and each element array is filled up with 5m of resins of a translucency, and is solidified, and a resin mould is carried out Drawing 8 shows the state at the time of ending this resin mould process. Like illustration, the space between each element array in drawing 7 is filled up with 5m of resins, and the mould object of a rectangular parallelepiped is made as a whole. In addition, the upper surface (and/or, inferior surface of tongue) of the mould object in the state of drawing 8 needs to maintain the cutting plane of each element array when taking arrangement of drawing 7 , i.e., to have exposed the edge cross section of a conductive layer 2 in the cutting plane of the element array cut down at the resin-seal substrate logging process. Therefore, what is necessary is just to perform the process (for example, based on polish) to expose to expose more certainly, when the conductive layer 2 exposed at the resin mould process is covered by 5m of resins.

[0017] (: refer to drawing 9 like an electric conduction metal membrane galvanizer) In addition to the electric conduction metal membrane 6, for example, a Cu-nickel alloy, this process prepares plating of flash plate gold all over the upper surface which the cutting plane of the insulating substrate 1 of the mould object of the shape of a rectangular parallelepiped acquired at the resin mould process of a last process exposes, and/or an inferior surface of tongue. At this time, the electric conduction metal membrane 6 contacts the conductive layer 2 exposed to the upper surface (and/or, inferior surface of tongue) of a mould object, and between both connects conductively.

[0018] (Electric conduction metal membrane removal process : refer to drawing 10) This process is a process which removes an unnecessary portion from the

plating side performed like the front electric conduction metal membrane galvanizer. Since the electric conduction metal membrane 6 is plated with the front process all ov r the upper surface (and/or, inferior surface of tongue) of a rectangular parallelepiped-like mould object, the conductive layer 2 of the couple which was connected electrically and which counters has each Light Emitting Diode element 3 in the state where it flowed by this electric conduction metal membrane 6. Then, the conductive layer 2 of the couple which each Light Emitting Diode element 3 of each element array counters is separated at once by removing beltlike ** for the electric conduction metal membrane 6 by etching, polish, etc. That is, since the node with the conductive layer 2 of each Light Emitting Diode element 3 by the side of the element array which the element array is aligned at the previous process and connected with the electric conduction metal membrane 6 is located in a line on the straight line, as shown in drawing 10 which shows the state where this process finished, it leaves the electric conduction metal membrane 6 to band-like lengthwise, and the other portion is removed.
[0019] (Dicing process : refer to drawing 11) This process performs element division by the dicer at the process divided into each parts as a side luminescence type chip Light Emitting Diode. About lengthwise, the chip Light Emitting Diode shown in drawing 1 or 3 can be obtained by making into a cutline the center of the width of face of the electric conduction metal membrane 6 which it left to band-like at the last process, and cutting a position in an equal pitch also about a longitudinal direction. Here, since the center of the width of face of the electric conduction metal membrane 6 formed like the galvanizer is made into a cutline and division into each chip Light Emitting Diode is performed, arrangement of the electrode by the electric conduction metal membrane 6 in the vertical side where the chip Light Emitting Diode after division faces each other will take arrangement along both ends, and brings about the feature as shown in the structure of Chip Light Emitting Diode drawing 1 or 3.
[0020]
[Effect of the Invention] According to this invention, the end face of an insulating substrate is exposed on the superficies of the resin mould object of an assembly which put the element on the edge at the insulating substrate which has a conductive layer with the aforementioned conductive layer. By forming an electrode in the superficies of a resin mould object so that a part or all of a conductive layer that was exposed may be included, secure conductive connection of an electrode and a conductive layer, and chip electronic parts are written as the composition corresponding to mounting every width. Since the electrode formed in the inferior surface of tongue of a resin mould object contacts the circuit pattern side by the side of a mother board in fields when chip electronic parts are mounted sideways, installation intensity and electrical installation are fully secured. Furthermore, when making connection according an electrode and wiring to solder by contact of fields, the problem that standing up of a chip occurs for example, in the conventional side luminescence type chip Light Emitting Diode by the position precision, faulty connection, or the Manhattan phenomenon after the installation which was a problem does not arise from self-alignment working at the time of soldering. Moreover, when mounting to the edge of a mother board often applies

this invention to the required side luminescence type chip Light Emitting Diode, it becomes possible to lessen defluxion of the chip by the imperfect connection which had broken out when the conventional side luminescence type chip Light Emitting Diode was mounted. Moreover, side type chip electronic parts equipped with the aforementioned feature can be created easily and efficiently by the method of this invention.

[Translation done.]

* NOTICES *

TECHNICAL FIELD

[The technical field to which invention belongs] this invention can be especially applied more to a detail about side type chip electronic parts about the chip electronic parts which come to form an electrode in a front face and its manufacture method of a resin mould object of chip electronic parts effective in optical semiconductor devices, such as Light Emitting Diode, a photo coupler, and a photo transistor, for example.

[Translation done.]

PRIOR ART

[Description of the Prior Art] A perspective diagram shows one example of the conventional side luminescence type chip Light Emitting Diode to drawing 12 . In drawing 12 , the side luminescence type chip Light Emitting Diode 20 is in the state where attached to the mother board 21 and it laid in the state of carrying out side luminescence. Side luminescence type chip Light Emitting Diode20 themselves are wearing a part of field which the Light Emitting Diode element 13 of an insulating substrate 11 lays by the closure resin 15 with the function for mounting the Light Emitting Diode element 13 which has a semiconductor luminous layer on the electrode 12 which consists of an electric conduction film by which patterning was mostly carried out to the whole surface of the rectangular parallelepiped-like insulating substrate 11, and protecting the Light Emitting Diode element 13 further, and drawing light in the predetermined direction. As for the electrode structure of the substrate adopted in the conventional example of illustration, the electrode 12 is formed in the 4 sides ranging from the field to the rear face where the Light Emitting Diode element 13 is mounted. And solder connection of the electrode 12 of the ends of an insulating substrate 11 is made so that it may become perpendicular to a mother board 21 about the field where the Light Emitting Diode element 13 of a substrate 11 is mounted. Therefore, an electrode does not exist in the field of the substrate 11 which faces the mother board 21 of a chip Light Emitting Diode 20. This is because each chip is started by dicing, and the started field is mounted so that a mother board 21 may be faced after forming the electrode for two or more chips in the circumference side of the insulating substrate of one sheet.

[0003] Thus, with the conventional electrode structure, installation intensity is weak and there is a danger that omission of a chip will occur by contact. The danger that omission etc. will occur by contact especially while dealing with the board, since it is attached in the edge of a mother board in many cases in the case of the side luminescence type chip Light Emitting Diode is high. Furthermore, since the electrode is not prepared in the field by the side of the chip Light Emitting Diode to the wiring side of a mother board, the problem that self-alignment does not work, and the position precision after installation does not come out, or a faulty connection occurs at the time of soldering, and the problem that soldering is impossible in the case of a small chip, or a chip stands up by the Manhattan phenomenon arise.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] According to this invention, it is the aforementioned conductive layer about the end face of an insulating substrate to the superficies of the resin mould object of an assembly which put the element on the edge at the insulating substrate which has a conductive layer. Secure conductive connection of an electrode and a conductive layer by forming an electrode in the superficies of a resin mould object so that a part or all of a conductive layer that was made to expose and was exposed may be included, and chip electronic parts are written as the composition corresponding to mounting every width. Since the electrode formed in the inferior surface of tongue of a resin mould object contacts the circuit pattern side by the side of a mother board in fields when chip electronic parts are mounted sideways, installation intensity and electrical installation are fully secured. Furthermore, when making connection according an electrode and wiring to solder by contact of fields, the problem that standing up of a chip occurs for example, in the conventional side luminescence type chip Light Emitting Diode by the position precision, faulty connection, or the Manhattan phenomenon after the installation which was a problem does not arise from self-alignment working at the time of soldering. Moreover, when mounting to the edge of a mother board often applies this invention to the required side luminescence type chip Light Emitting Diode, it becomes possible to lessen defluxion of the chip by the imperfect connection which had broken out when the conventional side luminescence type chip Light Emitting Diode was mounted. Moreover, side type chip electronic parts equipped with the aforementioned feature can be created easily and efficiently by the method of this invention.

[Translation done.]

* NOTICES *

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] this invention is made in view of the trouble in the conventional side type chip electronic parts mentioned above, installation intensity and electrical installation are secured and the purpose is in offering the aforementioned chip electronic parts with structure which self-alignment commits at the time of soldering, and its manufacture method, when making mounting connection of the aforementioned electronic parts at a mother board.

[Translation done.]

* NOTICES *

MEANS

[Means for Solving the Problem] Invention of a claim 1 mounts a semiconductor device on the insulating substrate which prepared the conductive layer, is the element mould object which carried out the resin seal of the semiconductor device to this insulating substrate, and constitutes the chip electronic parts which have the element mould object which the end face of this insulating substrate exposes to the superficies with a part of conductive layer, and the electrode prepared so that it might connect conductively to the superficies of the aforementioned element mould object at the aforementioned conductive layer.
[0006] Invention of a claim 2 is characterized by considering as the side of the aforementioned element mould object in which the abbreviation perpendicular was made to the field of the aforementioned insulating substrate where the aforementioned semiconductor device was mounted in the field in which the aforementioned electrode is prepared in chip electronic parts according to claim 1.
[0007] Invention of a claim 3 is characterized by making into a semiconductor light emitting device the element mounted on the aforementioned insulating substrate in side type chip electronic parts according to claim 1 or 2.
[0008] Invention of a claim 4 forms the repeat pattern of the unit pattern of the conductive layer of the configuration according to the semiconductor device in an insulating substrate. The resin mould of the semiconductor device which assembled two or more semiconductor devices to the insulating substrate in which the aforementioned pattern was formed, and was assembled to the aforementioned insulating substrate and this insulating substrate is carried out. Logging which this mould object is cut [logging] and exposes the edge cross section of the aforementioned pattern to the cutting plane is performed. Carry out the resin mould of the mould object which has arranged the cutting plane containing the edge cross section of the pattern exposed by the aforementioned logging to the same field, and was cut down from the aforementioned mould object further, and an element mould object is formed. An electric conduction metal is plated all over the aforementioned cutting plane arranged in this element mould object in the same side being included. The manufacture method of the chip electronic parts which carry out patterning removal of the plating portion unnecessary from the field which gave the aforementioned plating, and are characterized by dividing into each chip electronic parts the element mould object which performed patterning removal of the aforementioned plating is constituted.

[0009]
[Embodiments of the Invention] Hereafter, it explains based on the drawing which appends the gestalt of operation of the chip electronic parts by this invention, and its manufacture method. Drawing 1 shows the appearance of the side luminescence type chip Light Emitting Diode of the example of 1 operation gestalt of the chip electronic parts by this invention with a perspective diagram. Moreover, drawing 2 and drawing 3 show the plan and side elevation of the side luminescence type chip Light Emitting Diode which are shown in drawing 1 , respectively. one conductive-layer 2 top of the plane view rectangle-like insulating substrate 1 which formed the conductive layers 2 and 2 of the couple to which the chip Light Emitting Diode of this operation gestalt counters both ends, and an insulating substrate 1 -- an inferior surface of tongue -- a conductor -- as it mounts with a paste, and the Light Emitting Diode element 3 to which the upper surface was electrically connected with the conductive layer 2 and wire 4 of another side is closed by the epoxy resin 5 and shown in drawing 1 , the resin mould object which fabricated the whole in the rectangular parallelepiped mostly is made Here, that a side luminescence type should be constituted (drawing 1 is in a side luminescence state, and shows the luminescence direction by the arrow of illustration), the substrate 1 which mounts the Light Emitting Diode element 3 is set in a relation parallel to the side used as a luminescence side so that the side of a resin mould object may turn into a luminescence side, and an element mould object is fabricated.
[0010] Moreover, an electrode 6 is formed in the front face of an element mould object. As shown in drawing 1 or 3, in order to carry out bonding to the wiring by the side of a mother board (not shown), arrangement of an electrode 6 considers as the vertical side (namely, vertical side over the side in which a luminescence side is made) of an element mould object, and is arranged in this operation gestalt along the both ends of the vertical side which faces each other. Thus, you have to connect the conductive layer 2 of an insulating substrate 1 conductively to the electrode 6 prepared. The connection method is performed by forming an electrode 6 in the field containing the conductive layer 2 to which it was made to expose to the vertical side of an element mould object with the end face of an insulating substrate 1, and the conductive layer 2 prepared in the insulating substrate 1 was exposed. In addition, although the electrode 6 is formed in vertical both sides of a resin mould object with this operation gestalt; when carrying a single Light Emitting Diode element, one pair of electrode should just be in one of fields fundamentally. Moreover, when it is necessary to choose polarity and to mount on a mother board, a common electrode is prepared in vertical both sides, respectively, and a field is chosen and used.
[0011] Since the above-mentioned side luminescence type chip Light Emitting Diode has prepared the electrode for the two poles of a size required for the inferior surface of tongue of a resin mould object, when carrying out bonding to the wiring by the side of a mother board, two electrodes will contact the circuit pattern side by the side of a mother board in fields. Therefore, since installation intensity and electrical installation are fully secured and self-alignment works in the case of soldering, position precision can be taken out, neither a faulty connection nor the

problem that standing up of a chip occurs by the Manhattan phenomenon occurs, and the reliability of soldering improves. Moreover, in the side luminescence type chip Light Emitting Diode which needs mounting to the edge of a mother board, defluxion of the chip by the contact which had occurred since the conventional imperfect connection method was taken can be lost.

[0012] Next, the explanation is given to below about the method of creating the side luminescence type chip Light Emitting Diode shown above as 1 operation gestalt of the manufacture method of the chip electronic parts by this invention. Drawing 4 or drawing 11 is drawing for explaining the outline of this operation gestalt, and is drawing which expresses in order the state of the chip Light Emitting Diode processed and processed in creation process. In addition, drawing 1 , or 3 and a common reference number is given to the component of Chip Light Emitting Diode all over this drawing. Based on drawing 4 or drawing 11 , it explains in detail according to the process of creation of the side luminescence type chip Light Emitting Diode of this operation gestalt below. In addition, although this operation gestalt shows the example in which the conductive layer 2 was formed only on one side of an insulating substrate 1 as shown in drawing 4 , you may form so that both sides of a substrate 1 may be covered through the side, and a Light Emitting Diode element can also be assembled to both sides of a substrate 1 in this case.

[0013] At the process assembled to an insulating substrate 1, the Light Emitting Diode element 3 (: refer to drawing 4 like an element erector) In this example In each element mounting section of the conductive layer 2 for two or more chips which aligned on the insulating substrate 1 at length and the longitudinal direction and which is repeatedly formed in the pattern array It is the process which carries out die bonding of the Light Emitting Diode element 3 with a silver paste etc., and performs wirebonding with the wire 4 of a gold streak further between another electrode of the Light Emitting Diode element 3, the aforementioned mounting section, and the conductive layer 2 that counters.

[0014] (Resin-seal process : refer to drawing 5) At this process, the mould of the circumference of the Light Emitting Diode element 3 on the insulating substrate 1 assembled at the last process and the wire 4 which carried out bonding is carried out by the resin of a translucency, and the Light Emitting Diode element 3 and wire 4 portion are closed at least. The state at the time of ending this resin-seal process is shown in drawing 5 . Here, the resin 5 which carried out the mould of the circumference of the Light Emitting Diode element 3 and the wire 4 which carried out bonding stood in a row in height fixed in the shape of heights in a longitudinal direction, and in order not to carry out the resin mould of between the heights of a resin 5, the conductive layer 2 has exposed it.

[0015] (Resin-seal substrate logging process : refer to drawing 6) This process is a process which starts the substrate closed at the front resin-seal process, cuts the middle (A-A dashed line of drawing 5) of an element array, and cuts down a bar-like element array so that the circumference of the Light Emitting Diode element 3 which needed closure at the resin-seal process along with the lengthwise array of a conductive layer 2 using meanses, such as a dicer, and the wire 4 which carried out bonding may be saved. Drawing 6 shows the state at the

time of ending this resin-seal substrate logging process. Like illustration, at a last process, since the conductive layer 2 forms the repeat pattern so that the gestalt of a continuation pattern may be taken in length and a longitudinal direction, the conductive layer 2 which was continuing between the elements 3 on a par with a longitudinal direction by this logging is separated, and the edge cross section of a conductive layer 2 is exposed.

[0016] (Resin mould process : refer to drawing 7 and drawing 8) This process is a process which rearranges the element array cut down at the front resin-seal substrate logging process, and carries out the resin mould of the whole. At this process, first, as are shown in drawing 7 , and each cut-down element array is carried out every width, and the cutting plane of each element array is put on a coplanar and each element array is further aligned in the unit of an element lengthwise, each element array is piled up and rearranged. thus, such [the degree which enables division by the dicing to each chip Light Emitting Diode later mentioned by arranging] an array — maintaining — the upper and lower sides — fabrication — metal mold (not shown) — binding tight — fabrication — the cavity made with metal mold and each element array is filled up with 5m of resins of a translucency, and is solidified, and a resin mould is carried out Drawing 8 shows the state at the time of ending this resin mould process. Like illustration, the space between each element array in drawing 7 is filled up with 5m of resins, and the mould object of a rectangular parallelepiped is made as a whole. In addition, the upper surface (and/or, inferior surface of tongue) of the mould object in the state of drawing 8 needs to maintain the cutting plane of each element array when taking arrangement of drawing 7 , i.e., to have exposed the edge cross section of a conductive layer 2 in the cutting plane of the element array cut down at the resin-seal substrate logging process. Therefore, what is necessary is just to perform the process (for example, based on polish) to expose to expose more certainly, when the conductive layer 2 exposed at the resin mould process is covered by 5m of resins.

[0017] (: refer to drawing 9 like an electric conduction metal membrane galvanizer) In addition to the electric conduction metal membrane 6, for example, a Cu-nickel alloy, this process prepares plating of flash plate gold all over the upper surface which the cutting plane of the insulating substrate 1 of the mould object of the shape of a rectangular parallelepiped acquired at the resin mould process of a last process exposes, and/or an inferior surface of tongue. At this time, the electric conduction metal membrane 6 contacts the conductive layer 2 exposed to the upper surface (and/or, inferior surface of tongue) of a mould object, and between both connects conductively.

[0018] (Electric conduction metal membrane removal process : refer to drawing 10) This process is a process which removes an unnecessary portion from the plating side performed like the front electric conduction metal membrane galvanizer. Since the electric conduction metal membrane 6 is plated with the front process all over the upper surface (and/or, inferior surface of tongue) of a rectangular parallelepiped-like mould object, the conductive layer 2 of the couple which was connected electrically and which counters has each Light Emitting Diode element 3 in the state where it flowed by this electric conduction metal

membrane 6. Then, the conductive layer 2 of the couple which each Light Emitting Diode element 3 of each element array counters is separated at once by removing beltlike ** for the electric conduction metal membrane 6 by etching, polish, etc. That is, since the node with the conductive layer 2 of each Light Emitting Diode element 3 by the side of the element array which the element array is aligned at the previous process and connected with the electric conduction metal membrane 6 is located in a line on the straight line, as shown in drawing 10 which shows the state where this process finished, it leaves the electric conduction metal membrane 6 to band-like lengthwise, and the other portion is removed.
[0019] (Dicing process : refer to drawing 11) This process performs element division by the dicer at the process divided into each parts as a side luminescence type chip Light Emitting Diode. About lengthwise, the chip Light Emitting Diode shown in drawing 1 or 3 can be obtained by making into a cutline the center of the width of face of the electric conduction metal membrane 6 which it left to band-like at the last process, and cutting a position in an equal pitch also about a longitudinal direction. Here, since the center of the width of face of the electric conduction metal membrane 6 formed like the galvanizer is made into a cutline and division into each chip Light Emitting Diode is performed, arrangement of the electrode by the electric conduction metal membrane 6 in the vertical side where the chip Light Emitting Diode after division faces each other will take arrangement along both ends, and brings about the feature as shown in the structure of Chip Light Emitting Diode drawing 1 or 3.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the perspective diagram showing 1 operation gestalt of the side luminescence type chip Light Emitting Diode by this invention.
[Drawing 2] It is the plan of the side luminescence type chip Light Emitting Diode shown in drawing 1 .
[Drawing 3] It is the side elevation of the side luminescence type chip Light Emitting Diode shown in drawing 1 .
[Drawing 4] Drawing explaining the manufacturing process of the side luminescence type chip Light Emitting Diode shows the state of the product which can be set like an element erector.
[Drawing 5] Drawing explaining the manufacturing process of the side luminescence type chip Light Emitting Diode shows the state of the product in a resin-seal process.
[Drawing 6] Drawing explaining the manufacturing process of the side luminescence type chip Light Emitting Diode shows the state of the product in a resin-seal substrate logging process.
[Drawing 7] Drawing explaining the manufacturing process of the side luminescence type chip Light Emitting Diode shows the arrangement state of the element array in a resin mould process.
[Drawing 8] Drawing explaining the manufacturing process of the side luminescence type chip Light Emitting Diode shows the state of the product which can be set like an electric conduction metal membrane galvanizer.
[Drawing 9] Drawing explaining the manufacturing process of the side luminescence type chip Light Emitting Diode shows the state of the product in an electric conduction metal membrane removal process.
[Drawing 10] Drawing explaining the manufacturing process of the side luminescence type chip Light Emitting Diode shows the state of the product in an electric conduction metal membrane removal process.
[Drawing 11] Drawing explaining the manufacturing process of the side luminescence type chip Light Emitting Diode shows the state of the product in a dicing process.
[Drawing 12] It is the perspective diagram showing one example of the conventional side luminescence type chip Light Emitting Diode in the state of mounting to a mother board.

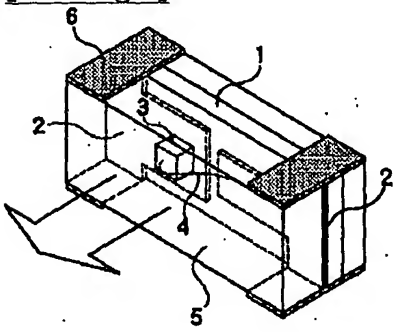
[Description of Notations]
1 11 — Insulating substrate
2 12 — Conductive layer
3 13 — Light Emitting Diode element,
4 — Wire
5 15 — Resin
6 — Electrode (electric conduction metal membrane),
20 — Side luminescence type chip Light Emitting Diode
21 — Mother board.

[Translation done.]

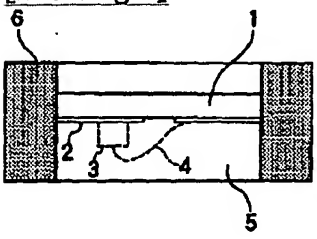
* NOTICES *

DRAWINGS

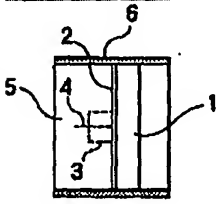
[Drawing 1]



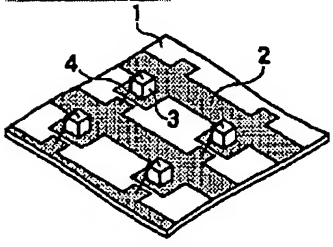
[Drawing 2]



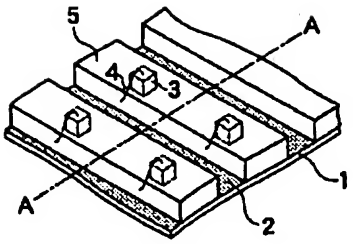
[Drawing 3]



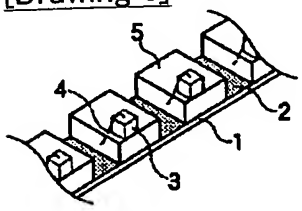
[Drawing 4]



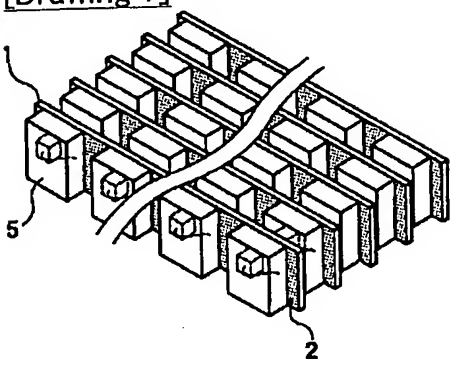
[Drawing 5]



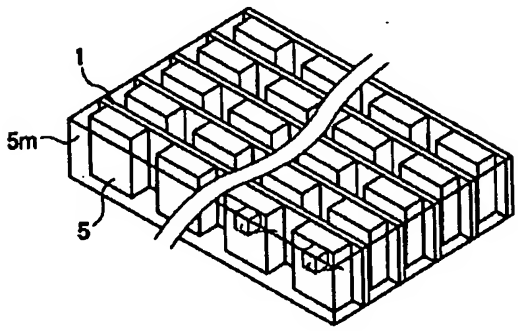
[Drawing 6]



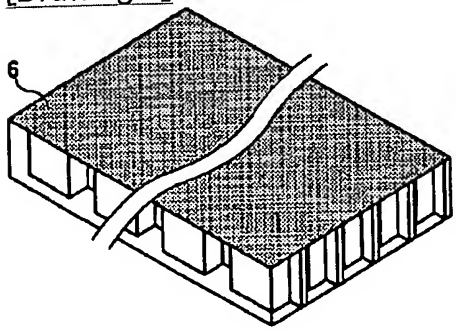
[Drawing 7]



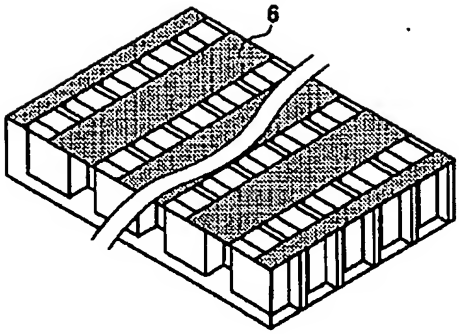
[Drawing 8]



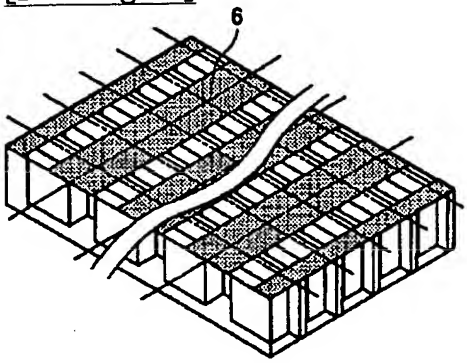
[Drawing 9]



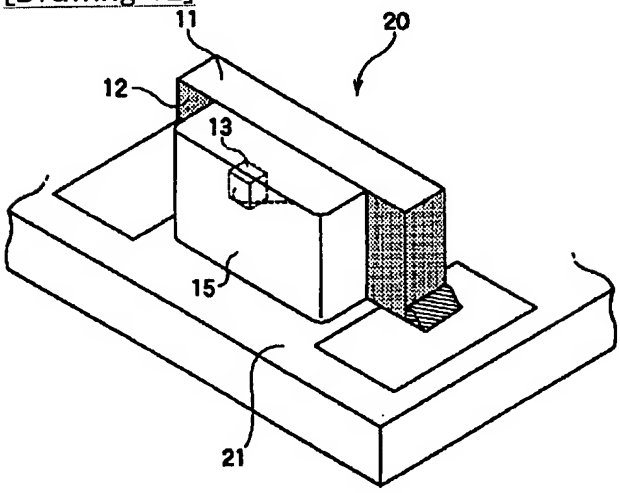
[Drawing 10]



[Drawing 11]



[Drawing 12]



[Translation done.]